Amendments to the Claims:
This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of fabricating an integrated silicon-germanium heterobipolar transistor wherein between a silicon-germanium base layer and a silicon emitter layer a silicon dioxide layer is formed, characterized in that said silicon dioxide layer is formed by means of Rapid Thermal Processing (RTP), wherein said base layer is heated in a sequence of temperature steps to a process temperature at which said silicon dioxide layer is subsequently formed and wherein in a first temperature step said base layer is heated to a temperature between 350°C and 500°C.

2. (original) The method as set forth in claim 1 wherein said silicon dioxide layer and said emitter layer are formed by means of a single continual process.

3-4. (cancelled)

5. (currently amended) The method as set forth in claim [[4]]1 wherein said base layer is heated in a second temperature step to approximately 640°C.

6. (original) The method as set forth in any of the claims 5 wherein said base layer 15 is heated in a third temperature step to approximately 705°C.

7. (currently amended) The method as set forth in claim [[3]]1 wherein said base layer is heated in a nitrogen atmosphere.

8. (cancelled)

9. (original) The method as set forth in claim 1 wherein said base layer 20 is exposed to an oxygen-nitrogen atmosphere for approximately 10 seconds.

10. (original) The method as set forth in claim 1 wherein said silicon dioxide layer has a thickness between 0.3 nm and 0.4 nm, preferably approximately 0.35 nm.

11. (original) The method as set forth in claim 1 wherein said silicon-germanium heterobipolar transistor is a pnp-bipolar transistor.

12. (original) The method as set forth in claim 1 wherein an emitter layer is formed of polysilicon.

13. (original) The method as set forth in claim 1 wherein the properties of said silicon dioxide layer are monitored during said RTP.

14. (original) The method as set forth in claim 1 wherein the surface of said silicon-germanium base layer is pre-cleaned and said silicon dioxide layer is subsequently formed in a single continual process.

15-16. (cancelled).

17. (new) A method of fabricating an integrated circuit comprising the steps of:

forming a silicon-germanium base layer on a wafer;

transferring the silicon-germanium base layer to a Rapid Thermal Oxidation (RTO) chamber;

heating the silicon-germanium base layer using a sequence of temperature steps in the RTO chamber;

forming a silicon dioxide layer over the silicon-germanium base layer in said RTO chamber

transferring the silicon-germanium base layer from the RTO chamber after forming the silicon dioxide layer; and

forming a silicon emitter layer over the silicon dioxide layer.

18. (new) The method of claim 17, wherein said sequence of temperature steps comprises:

a first temperature step heating to a first temperature;

a second temperature step heating to a second temperature higher than said first temperature; and

a third temperature step heating to a third temperature higher than said second temperature.

19. (new) The method of claim 18, wherein said first temperature is in the range of 350°C to 500°C.

20. (new) The method of claim 18, wherein said second temperature step comprises relatively quickly heating to the second temperature.

21. (new) The method of claim 18, wherein the second temperature is approximately 640°C.

22. (new) The method of claim 18, wherein said third temperature step comprises relatively slowly heating to the third temperature.

23. (new) The method of claim 18, wherein the third temperature is approximately 705°C.

24. (new) The method of claim 17, wherein said sequence of temperature steps comprises:

heating to a first temperature in the range of 350°C to 500°C;

relatively quickly heating to a second temperature higher than the first temperature; and

relatively slowly heating to a third temperature higher than said second temperature.